a)

A[n-1:0]   B[n-1:0]   input operands

Booth recoder radix 4

selection logic

• • •

partial product reduction
(n+1)/2 : 2

PC[2n-1:0] PS[2n-1:0]   product in
carry-save
representation

b)

A[n-1:0]   B[n-1:0]   input operands

3x

Booth
recoder
radix 8

selection logic

• • •

partial product reduction
(n+1)/3 : 2

PC[2n-1:0] PS[2n-1:0]   product in
carry-save
representation

Figure 1: Block digrams of partial product generation for prior art a) Booth radix-4 and b) Booth radix-8 multipliers.

a)

A[n-1:0]   B[n-1:0]   input operands

7x

recoder
for
7x digits

recoder for
1x digits

selection logic

• • •

partial product
reduction
(n+1)/5 :4

selection logic   4:2

• • •

partial product reduction
(n+1)/5 +2 :2

PC[2n-1:0] PS[2n-1:0]   product in
carry-save
representation

b)

B[n-1:0]   input operand

recoder
for
7x digits

recoder
for
1x digits

A[n-1:0]   input operand

selection logic   selection logic

• • •   • • •

partial product
reduction
(n+1)/5 :2

partial product
reduction
(n+1)/5 :2

7x
computation

partial product reduction
6:2

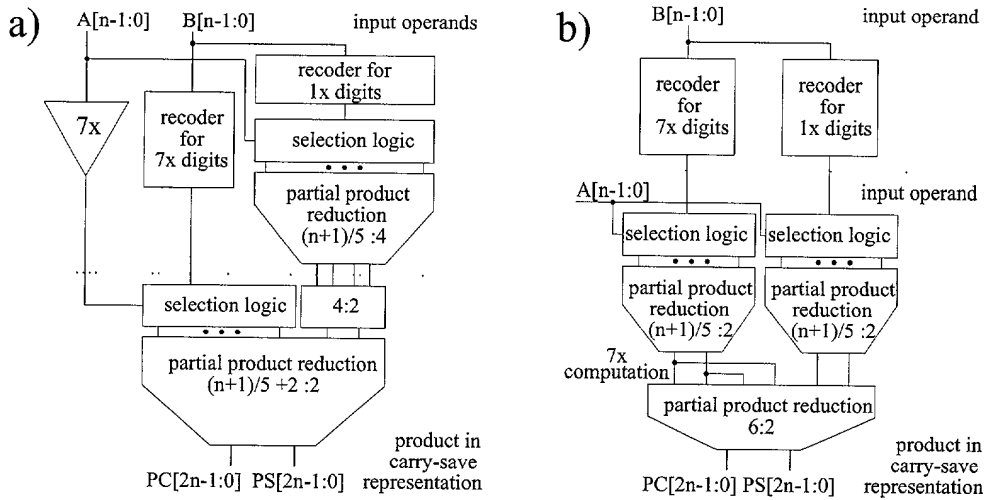PC[2n-1:0] PS[2n-1:0]   product in
carry-save
representation

Figure 2: Simplified block digrams of partial product generation for a) radix-32 recoding with precomputation of $7x$ and b) preferred embodiment radix-32 encoding with postcomputation of $7x$ multipliers.
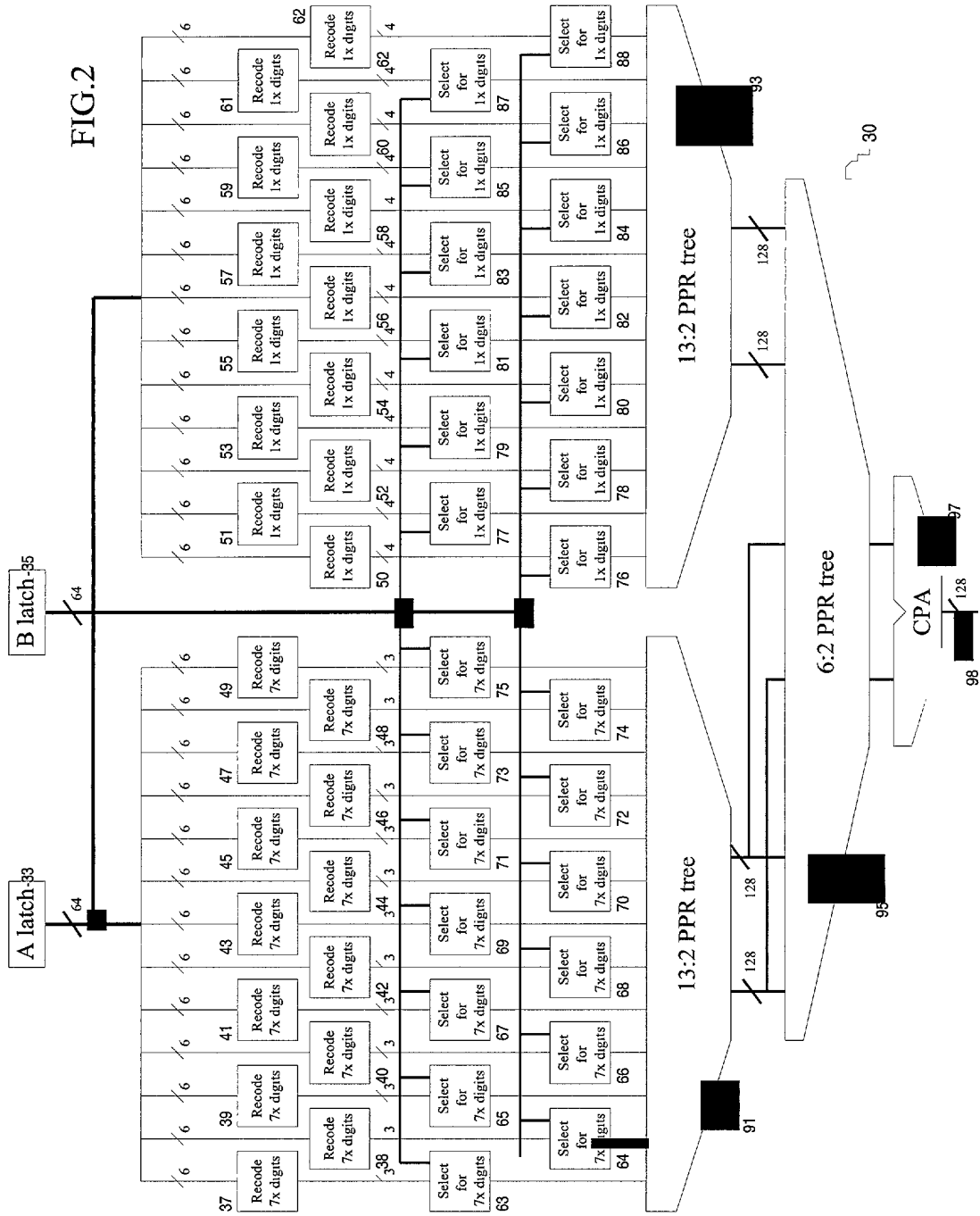
FIG.2

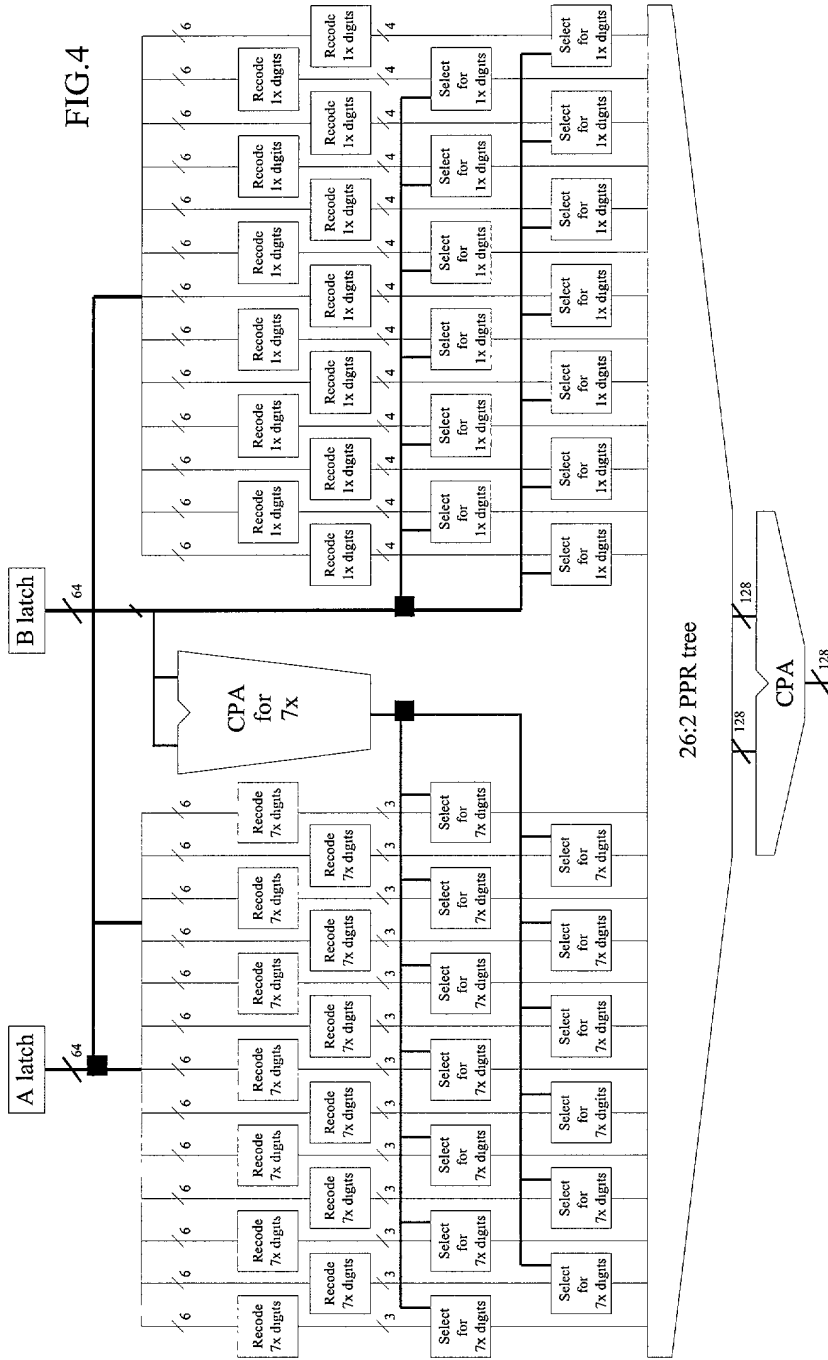Figure 3: Block diagram of the preferred embodiment of the invention for a multiplier bit width of $p = 64$.

Figure 4: Block diagram of the precomputation option illustrating a further embodiment of the invention for a multiplier bit width of $p = 64$.